Thrust IV: Low Power Systems on Chip

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3-Plane Diagram
Testbeds: HET and SAP – Thrust IV

HET Testbed
- Battery
- Environmental Sensor
- Physiological Sensor
- Power Management
- Digital Control / Processing / Management
- Analog Front End
- Software
- Antenna

SAP Testbed
- Energy Harvesting
- Physiological Sensor
- Energy Storage
- Power Management
- Digital Control / Processing / Management
- Analog Front End
- Software
- Antenna

Medical / Off Body
- Aggregator
- User Interface
- Signal Processing
- Smartphone
- IOIO
- Radio

Biocompatibility
COTS Add-on

Cloud Storage
Signal Processing
Thrust IV Goals / Specs: Testbed-Driven

- SOC / Radios (already in Testbed talk)
  - Designed for testbed requirements
  - Meet testbed specifications
- Cross-disciplinary Research
- Field-leading Accomplishments
  - Clock generation
  - Antenna design
  - Chip-chip I/O
Approach: Cross Disciplinary Research, Driven by Testbeds

- Antenna + Radio (PSU + UVA); later this talk
- TEG + boost converter (NC SU + UVA); earlier today
- TFETS + SOC (PSU + UVA); Thrust II talk
- Gas sensor + chip (PSU + UVA); Thrust III talk
## Selected Testbed Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Spec</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SoC, incl. active RF</td>
<td>Power</td>
<td>10</td>
<td>µW</td>
</tr>
<tr>
<td>ECG Sensor</td>
<td>Power</td>
<td>3</td>
<td>µW</td>
</tr>
<tr>
<td>Accelerometer</td>
<td></td>
<td>5</td>
<td>µW</td>
</tr>
<tr>
<td>Total System</td>
<td></td>
<td>&lt;30</td>
<td>µW</td>
</tr>
<tr>
<td>Clock generation</td>
<td>XTAL frequency</td>
<td>32</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Power</td>
<td>10</td>
<td>nW</td>
</tr>
<tr>
<td></td>
<td>Stability</td>
<td>5</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>Antenna</td>
<td>Tx/Rx Frequency</td>
<td>4 / 2.4</td>
<td>GHz</td>
</tr>
<tr>
<td></td>
<td>S11 in band</td>
<td>&lt; -10</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>gain</td>
<td>5 - 8</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>efficiency</td>
<td>&gt;75</td>
<td>%</td>
</tr>
<tr>
<td>Chip-to-Chip IO</td>
<td>Datarate</td>
<td>1 to 500</td>
<td>Kbps</td>
</tr>
<tr>
<td></td>
<td>Power</td>
<td>&lt; 0.5</td>
<td>µW</td>
</tr>
</tbody>
</table>
Thrust IV Goals / Specs: Testbed-Driven

- SOC / Radios (already in Testbed talk)
- Cross-disciplinary Research
- Field-leading Accomplishments: 3 Research Examples
  - Clock generation
  - Antenna design
  - Chip-chip I/O
Deep Dive: ULP Crystal (XTAL)

- Testbeds: Clock is critical
- Runs all the time
- **PROBLEM**: 1st SoC: 19µW total, 2 µW for the clock crystal!

- **TESTBED NEED**: lower power with stability
- Approach: prototype a new chip

Shrivastava, Akella, Calhoun, UVA
Deep Dive: ULP Crystal (XTAL) (2)

**a) Measured power consumption of XTAL with $V_{DD}$, 27°C, w/ and w/o duty-cycling shows minimum power of 1.5nW**

**b) Measured minimum power consumption histogram of XTAL at 0.3V $V_{DD}$, 27°C, w/o duty-cycling across 25 chips**

Measured start-up of crystal oscillator at 0.4V $V_{DD}$

Measured duty-cycling operation of crystal oscillator

Output of clock buffer operating at 32.768 KHz with duty-cycling,

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Shrivastava, Akella, Calhoun, UVA

**1.5 nW power!**

**Good performance across variations: 1 part at 840pW!**
# Deep Dive: ULP XTAL Benchmarking

<table>
<thead>
<tr>
<th></th>
<th>ISSCC14</th>
<th>ISSCC12</th>
<th>ESSCIRC99</th>
<th>ISSCC94</th>
<th>This work</th>
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</thead>
<tbody>
<tr>
<td><strong>Operating Frequency</strong></td>
<td>32kHz</td>
<td>32kHz</td>
<td>32 kHz</td>
<td>32kHz</td>
<td>32kHz</td>
</tr>
<tr>
<td><strong>Area (mm²)</strong></td>
<td>0.03</td>
<td>0.3</td>
<td>N/A</td>
<td>25</td>
<td>0.0625</td>
</tr>
<tr>
<td><strong>Power Consumption (nW)</strong></td>
<td>1.89</td>
<td>5.58</td>
<td>22</td>
<td>220</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>Operating $V_{DD}$(V)</strong></td>
<td>0.15-0.5</td>
<td>0.92-1.8</td>
<td>0.71</td>
<td>3</td>
<td>0.3</td>
</tr>
<tr>
<td><strong>Number of Power/Gnd</strong></td>
<td>1/1</td>
<td>2/2</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
</tr>
<tr>
<td><strong>Amplitude of Oscillation</strong></td>
<td>N/A</td>
<td>100mV</td>
<td>65mV</td>
<td>N/A</td>
<td>200mV</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>28nm</td>
<td>0.18µm</td>
<td>2µm</td>
<td>2µm</td>
<td>0.13µm</td>
</tr>
</tbody>
</table>

*World record*
Deep Dive: Antenna – Channel Characterization

Tested several custom prototype antennas on body
Compared with a commercially available antenna:
- The Rx antenna was fixed at different distances (1m, 2m) away from the person.
- The Tx antenna was mounted on the right chest, right upper arm, right waist, right wrist.
- 3 gestures and 4 body orientations were included in the tests.
- 5 antennas were tested: commercial 2.4 GHz, custom 2.4 GHz LP/CP, 4 GHz LP/CP.

Deep Dive: Antenna – Channel Characterization

Tested Transmit Antennas (Images are to scale) and Comparison

- Commercial 2.4 GHz
  - 94 x 82 mm² x 13 mm
  - Omnidirectional pattern
  - Low efficiency

- 2.4 GHz CP
  - 55 x 55 mm² x 5.5 mm
  - Unidirectional pattern
  - High efficiency
  - Circular polarization (robust to movement)

Werner (PSU)

50X more power efficient!

The custom designed antenna provides a much better wireless link than the COTS antenna

* Details are available in poster.
Deep Dive: Antenna (2) - Wideband Metasurface-based Wearable Antennas

Metasurface ground layers allow significant size reduction, wide bandwidth and high gain.

- **Version 1**: Doubly interdigital capacitor loaded metasurface for linear polarization.

**Version 2**: A sawtooth slot pattern to achieve size reduction and circularly polarized radiation with wide bandwidth at 80-90% efficiency

World record: Meeting testbed specs

Deep Dive: Chip-chip I/O

**Testbed needs**: overcome barriers by moving to multi-chip design
- Shortens design cycles, allows component revisions, supports disparate technologies

**Problem**:  
- Chip-chip I/O could limit power  
- Prior art is for high speed

Low energy, but high speed and power

Lukas, Calhoun, ISCAS 2015
Deep dive: Chip-chip I/O (2) - Benchmarking

- Test chip to look at low energy/bit, low speed I/O
- **World record**: Lowest power and E/b reported
- **Game changer for test beds**

World record: 1 nW - over 1,000,000X savings

Lowest energy/b

*Lukas, Calhoun, ISCAS 2015*
Barriers and Responses

- Complicated designs, slow cycles, multiple components
  - New hire: Dr. Dilip Vasudevan, research scientist (UVA)
  - New tech: ULP chip-to-chip I/O, separate chip sensor AFEs, radios

- RF connectivity; On-body Communications
  - New tech: Antennas, RF IC design, asymmetric radios, interface to standards

- TEG output power
  - New tech: TEG materials and packaging, on body integration, heat sinks

- Power management across multiple blocks
  - New tech: SOC architecture overhaul, DSP
Looking Ahead

ASSIST SoC Roadmap:
- Target new architecture and $<1\mu W$ SoC core (merge with Thrust II, V)
- Suite of SoC companion chips: sensors, radios (merge with Thrust I, III)
- Increased integration of DSP, data and energy co-management (merge with Thrust I, V)

ASSIST RF Roadmap:
- Multimodal radios talking to standard compliant radios
- Flexible antennas for data and harvesting, co-designed with RF ICs
- Increased connectivity options: eg, mesh networks

SoC in more testbed demos
- TX to BLE
- RF + antennae on body
- Refine testbed integration
- Begin new SoC architecture

Prototypes of $<1\mu W$ SoC
- Antennas with flexible materials
- Multifunction antennas
- RF interaction with standards
- Suite of sensor IC companions with SOC
- Advanced DSP

Multimodal harvester
- ULP blood pressure, pulse ox
- Data correlation on chip
- Integration of new TFETs, NVP

Year 4
- SoC in more testbed demos
- TX to BLE
- RF + antennae on body
- Refine testbed integration
- Begin new SoC architecture

Year 5
- Prototypes of $<1\mu W$ SoC
- Antennas with flexible materials
- Multifunction antennas
- RF interaction with standards
- Suite of sensor IC companions with SOC
- Advanced DSP

Year 6+
- Multimodal harvester
- ULP blood pressure, pulse ox
- Data correlation on chip
- Integration of new TFETs, NVP
Conclusion – Thrust IV is...

- ... directed by Testbed needs
- ... highly cross-disciplinary and collaborative
- ... overcoming major barriers with field-leading results
- ... connected to industry
  - E.g., extra funding (Samsung, Tyco), collaboration and test support (Wireless Research Center, Twisthink), startups (PsiKick), wanting SoC dev kits
- ... meeting Center goals and supporting Center vision

Thank you.

Questions?