Project title: Design, Fabrication and Characterization of Heterojunction Tunnel Field Effect Transistors (HTFETs) and Related Circuits for Ultra Low-Power/Self-Powered Nanoelectronics

Team Members: Project Leaders: Suman Datta & Vijaykrishnan Narayanan
Graduate Students: Bijesh Rajamohan, Rahul Pandey & Huichu Liu

Statement of project goals: Our overarching goal is to develop n and p-channel complementary Tunnel FET device technologies for a variety of digital and mixed signal applications ranging from ultra low-power digital logic to low noise transconductance amplifiers to energy-efficient analog-to-digital converters to signal rectifiers, vital for self-powered health monitoring SOC’s. The targeted transistor prototypes should offer steep (sub-kT/q) switching slope and beat the so-called tyranny of kT/q Boltzmann limit, deliver higher drive current than sub- and near threshold CMOS. Operate under supply voltage below 350mV – all at very low off-state leakage current. Further, tunnel FETs should demonstrate high transconductance and output resistance at very low drain bias current - suitable for implementing ultra low-power analog circuit blocks.

The project's role in support of the strategic plan: Our project is in support of Gen-2 (TFET compact model development for both digital and analog functions including noise effect), and Gen-3 (TFET based prototype digital and analog circuits demonstration for digital accelerator and analog blocks).

Discussion of fundamental research, educational, or technology advancement barriers and the methodologies used to address them:

Invention and successful demonstration of an ultra low-power and high performance transistor technology for all forms of computing from self-powered health monitoring chips to mobile handsets to green datacenters remains a formidable quest. Inter-band tunnel transistor (TFET) has recently emerged out of a myriad of device candidates as a promising transistor architecture which, in theory, can beat state-of-the-art CMOS technology in terms of both power and performance. This is illustrated in Figure 1 which summarizes the results of a detailed benchmarking results conducted by Young and Nikonov of Intel Corporation (IEDM 2012). TFETs operate on the principle of gate modulated band to band or inter-band tunneling of source carriers into the channel which undergoes an energy filtering process and gives rise to sub-60mV/decade switching slope in its transfer characteristics. This allows tunnel FETs to operate under very low supply voltage, $V_{DD}$, and provide enhanced energy efficiency over CMOS. There are two fundamental breakthroughs yet to be demonstrated simultaneously that will eventually determine the success of TFETs as
viable replacement or augmentation of classical CMOS in self powered microsystems: a) **band-gap engineering of tunnel heterojunctions** to demonstrate high drive current and sub-\(kT/q\) switching in TFETs; b) **atomically precise control of interface defect states at high-\(\kappa\)/non-silicon interface** to demonstrate steep switching slope.

**Foreign Collaborations**
None

**Summer internship:**
To obtain the professional support in defining the ultra-low power advanced transistor landscape and create synergy on evaluating HTFET emerging technology, ASSIST student Huichu Liu spent 3 months at Global Foundries in Sunnyvale, CA, as a summer internship student to establish our knowledge and understanding of the capabilities of the state of the art CMOS transistors and evaluate emerging device options (including steep slope tunnel FETs).

**Achievements in Year 3 and Previous Years:**
In the past year, we specifically focused on the following:

a) Demonstrated extremely scaled high-k gate dielectrics with high quality electrical interfaces with arsenide (As) and antimonide (Sb) channels

b) Demonstrated complimentary ‘all III-V’ Het-rojunction Vertical Tunnel FET (HVTFET) with record performance at \(|V_{DS}|=0.5V\). The p-type TFET (PTFET) has \(I_{ON}=30\mu A/\mu m\) and \(I_{ON}/I_{OFF}=10^5\), whereas the n-type TFET (NTFET) has \(I_{ON}=275\mu A/\mu m\) and \(I_{ON}/I_{OFF}=3\times10^5\), respectively.

c) NTFET shows 55mV/decade switching slope (SS) beating the 60mV/dec Boltzmann limit for the first time, while PTFET shows 115mV/decade SS in pulsed mode measurement.

d) Energy-delay performance benchmarking shows 3-4x reduction in energy consumption over state of the art CMOS at equivalent delay.

TFETs are promising devices for realization of energy efficient transistors with sub-\(kT/q\) switching slope. Heterojunction TFET using mixed arsenide-antimonide materials can achieve high on-current \(I_{ON}\), high \(I_{ON}/I_{OFF}\) ratio, through source-side tunnel barrier height \(E_{b,eff}\) engineering. To implement energy-efficient complementary logic, both NTFETs and PTFETs need to be realized preferably in the same material system. This year, for the first time, we demonstrate complementary TFETs with high on-current, high \(I_{ON}/I_{OFF}\) in arsenide-antimonide material sharing the same metamorphic buffer layer. We demonstrate sub-\(kT/q\) switching slope (SS) for NTFETs.

The advantages of complimentary heterojunction vertical tunnel FET (HVTFET)-based FOI

![Figure 2](a) Schematic of complimentary PTFET and NTFET on common metamorphic buffer technology; (b) Starting hetero-structures, and (c) Cross-section TEM micrographs of fabricated devices
inverter over FinFET FO1 inverter are quantified from circuit layout and energy-delay performance perspective.

**Complementary Tunnel FET Fabrication:** Fig. 2(a) illustrates the schematic of complimentary HVTFTEs sharing a common metamorphic buffer. Figs. 2(b) and (c) depict the epitaxial heterostructures and the cross-sectional TEM micrographs of N and PTFETs, respectively. Due to the differences in channel composition (As vs. Sb), NTFET and PTFET employ separately optimized ZrO2 and HfO2 gate stacks, respectively.

![Figure 2](image)

**Figure 2** (a) Schematic of complimentary HVTFETs sharing a common metamorphic buffer. Figs. 2(b) and (c) depict the epitaxial heterostructures and the cross-sectional TEM micrographs of N and PTFETs, respectively.

**Gate Stack Development:** A primary bottleneck for steep slope III-V TFETs has been development of high-k dielectric/III-V channel interface with low interface trap density (Dit) and low leakage current. Particularly, in the case of antimonide (Sb) channel PTFET, the surface Fermi level movement is typically restricted due to high mid-gap Dit. For PTFET with GaAs0.35Sb0.65 channel, we achieve the highest accumulation capacitance density (Cacc) with a high temperature (250°C) plasma clean due to efficient desorption of native oxide, albeit with formation of elemental Sb which worsens interface state density, Dit, (Fig. 2(a)). Optimization of

![Figure 3](image)

**Figure 3** (a) CV characteristics of p-type GaAs0.35Sb0.65 MOSCAPs with 3.5 nm HfO2 with H2 plasma surface clean at various temperatures; (b) CV characteristics of optimized gate stack; (c) Dit extraction using Terman method. Gate leakage is shown in the inset.

![Figure 4](image)

**Figure 4** (a) CV characteristics of n-type In0.53Ga0.47As MOSCAPs with 4nm ZrO2 with N2 plasma/TMA clean; (b) Dit extraction using Terman method. Gate leakage for both 3nm and 4nm ALD ZrO2 is shown in the inset; (c) Fermi level movement from dotted peak conductance.
the H₂ plasma surface clean temperature with 3.5 nm thick HfO₂ gate di-electric leads to the thinnest CET = 1.2 nm (capacitance equivalent thickness) with lowest mid-gap Dit (Figs. 2(b,c)). We achieve efficient Fermi level movement between valence band and the mid-gap but sluggish movement away from mid-gap, as observed from the normalized conductance maps in Fig. 2(d). For NTFET with In₀.₆₅Ga₀.₃₅As channel we employ 4nm thick ZrO₂ high-k dielectric (Fig. 3(a-c)) and achieve CET of 1.1 nm [2] with low mid-gap Dit. The conductance peak maximum trace indicates efficient Fermi level movement with gate voltage. The dual gate stack approach is essential for realizing complimentary TFETs with high on-current, steep switching slope and high I₁₀Ν/Iₒff ratio.

![Figure 5](image)

Figure 5 (a) DC Transfer and Output characteristics of (a-c) P TFET and (d-f) NTFET. All measurements are at T=300K, except the additional T=77K data in (c) and (f). NDR is visible in NTFET and PTFET illustrating all the devise work on quantum mechanical tunneling principle

**Complementary Tunnel FET Characterization:** Experimental room temperature transfer (I DS-V GS), and output characteristics (I DS-V DS) for the fabricated PTFET and NTFET are shown in Fig. 4(a-f). GaAs₀.₃₅Sb₀.₆₅ channel PTFETs exhibit I₁₀Ν =30μA/μm at I₁₀Ν/Iₒff =10⁵. The PTFET output characteristics exhibit negative differential resistance (NDR) and saturation at low temperature (77K) due to the suppression of mid-gap Dit response. In₀.₆₅Ga₀.₃₅As channel NTFET shows I₁₀Ν =275μA/μm at I₁₀Ν/Iₒff =3×10⁵. The mid-gap Dit with slow trap response time causes the DC switching slope (SS) in the fabricated N and PTFETs to exceed the Boltzmann thermal limit of 60 mV/decade at room temperature. We perform pulsed I DS-V GS measurements on TFETs with input gate voltage pulse with rise time varying from 10μs down to 300 ns to evaluate SS under actual switching environment. Fig. 5(a-d) shows the improvement in switching characteristics for both N and PTFET due to suppressed response of slow mid-gap Dit. We achieve SS=55mV/decade for NTFET and SS=115mV/decade for PTFET at room temperature. The high I₁₀Ν with sub-kT/q SS demonstration for NTFET and high I₁₀Ν with improved SS demonstration in case of PTFET, is a direct consequence of engineering high-quality scaled gate dielectrics and tunnel barriers in the As-Sb system.
Figure 6 (a) Pulsed mode transfer and switching characteristics of (a-b) PTFET and (c-d) NTFET. All measurements at 300K

**Circuit level compact models of Tunnel FETs:** Fabricated Tunnel FETs were used to calibrate the device compact models. Assuming lower Dit than the experimentally obtained values, we obtain steep SS ~40 mV/decade for both P and NTFETs. The energy-delay metric of TFETs shows improved energy efficiency over state-of-the-art CMOS below 0.3V supply voltage. In collaboration with the NSF funded NEEDS Center, we have made available our Heterojunction compact models on the Nano-Hub. According to NEEDS researchers, the HTFET compact modeled has been downloaded over 700 times since its publication in Oct, 2014, making it a popular emerging device model in NEEDs (private communication with Prof. Mark Lundstrom of Purdue University).

**Summary of other relevant work being conducted within and outside of the ERC and how this project is different:**
There are no other groups working within ERC on similar topic. Around the world, there are several leading device groups that are actively working on the demonstration of steep slope Tunnel FETs in a variety of material systems that include silicon-germanium (IBM Research, UCLA), germanium (UC Berkeley/Sematech, IMEC), III-Vs (Lund University, Notre Dame, MIT, University of Tokyo, IMEC, UT Austin, UC Santa Barbara), bi-layer graphene (UT Austin, Purdue) and two dimensional transition metal di-chalcogenides (Purdue, UT Austin, Penn State). Our project differs from the rest in several aspects: a) unique vertical transistor configuration with self-aligned gate electrode geometry; b) unique design of p-channel TFET; d) strongly coupled device-circuit co-design activities for digital accelerators, mixed signal data converters, analog rectifiers as well as understanding of noise and variability. The goal of this research is to develop a holistic picture of the viability of TFETs for self-powered SOC platform.

**Plans for next year:**
We will focus on improving the performance of the p-channel Heterojunction TFET by i) improving the interface between the antimonide channel and high-k dielectric. The latter will be
enabled by the new plasma enhanced atomic layer deposition cluster tool capability fully operational at Penn State with in-situ metrology, which will allow researchers to integrate in-situ cleaning of antimonide surfaces. We will use experimental device results to calibrate and refine compact models for n- and p-channel TFETs (in collaboration with NEEDS center). These models will delivered to Narayanan to generate TFET based circuit blocks co-optimized for the non-volatile processor architecture. The circuit blocks will be provided to Calhoun group to design SOCs for ASSIST Gen 3 systems. A successful experimental demonstration of a high performance and steep switching slope (40mV/decade) n-channel and p-channel Hetj TFET will be a significant milestone in the field of post CMOS low power device technologies. We will also demonstrate proof-of-concept analog circuit such as a ultra-low power operational transconductance amplifier and RF rectifier. We will provide microwave parameters of fabricated TFET prototypes to the Wentzloff group to design TFET based radio blocks for ASSIST Gen 3 system.

Expected milestones and deliverables for the project:

- Demonstration of scaled channel length (<100nm) complementary Tunnel FETs
- Demonstration of n-channel Tunnel FETs with 40mV/decade sub kT/q operation
- Demonstration of p-channel Tunnel FET with 40mV/decade sub kT/q operation
- Demonstration of Tunnel FET based prototype digital circuits (inverters, oscillators, rectifiers, amplifiers) with improved energy efficiency over CMOS

Member company benefits:
Emerging III-V HTFET based digital and analog circuits can potentially achieve significant energy efficiency improvement and performance gain over the state-of-art sub-threshold CMOS to realize battery-less, intelligent electronic systems for various applications including wearable health monitoring SOCs..

Publications:
[1] Rajamohanen, B.; Pandey, R.; Chobpattana, V.; Vaz, C.; Gundlach, D.; Cheung, K.; Suehle, J.; Stemmer, S.; Datta, S., "0.5V Supply Voltage Operation of In0.65Ga0.35As/GaAs0.4Sb0.6 Tunnel FET," IEEE Electron Device Letters, vol 36, no 1, January 2015
[2] R. Pandey, H. Madan, H. Liu, V. Chobpattana, M. Barth, B. Rajamohanan, M. J. Hollander, T. Clark, K. Wang, J. H. Kim, D. Gundlach, K. P. Cheung, J. Suehle, R. Engel-Herbert, S. Stemmer and S. Datta, “Demonstration of p-type In0.7Ga0.3As/GaAs0.35Sb0.65 and n-type GaAs0.4Sb0.6/In0.65Ga0.35As Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic” (accepted 2015 Symposium on VLSI Technology, June, Kyoto, Japan)
Project title:
Exploring non-volatile processor architectures and Tunnel FET (TFET) circuits for self-powered and adaptive health wellness platforms

Team Members:
Project Leader: Dr. Vijaykrishnan Narayanan (PI)
Students: Kaisheng Ma, Huichu Liu

State of Project Goals:
Goal 1: Design of a simulation platform based on a non-volatile processor and TFET-based circuits that can guide the selection of the appropriate energy management circuits/policies and signal processing architecture to deploy for the various energy sources/sensors/algorithms being explored by other ASSIST researchers.
Goal 2: Design of a prototype system shown in Figure 1 to demonstrate the utility of the non-volatile logic and memory in self-powered health systems. The prototype system will include the non-volatile processor, energy harvester including TFET blocks, and power management strategies explored in Goal 1. This prototype will also help validate the simulation platform and facilitate design of next generation prototypes incorporating newer optimizations resulting from the simulation studies targeted in Goal 1

![Figure 1. The proposed prototype platform for non-volatile signal processing](image)

Project's Role in Support of the Strategic Plan:
This project is under the center testbed of “Self-Powered and Adaptive Low Power Platform”. This project explores the utility of emerging nanoscale devices – tunnel FETs (TFET) and ferroelectric FETs (FeFET) in enhancing the capabilities of self-powered, adaptive health platforms. The project will leverage TFET circuits for the power harvesting and management circuits and explore the use of ferroelectric FETs to enable data retention and forward progress in computations overcoming intermittent lack of power supply. Non-volatile memory and logic can also provide
the ability for almost instantaneous shutdown and recovery, providing energy-efficient (near) zero-
standby power modes for low duty cycle health applications. The project will result in prototyping
a health wellness platform based on a non-volatile processor with thermo-electric/solar energy
source and interfaced to ASSIST and COTS sensors.

Discussion of Fundamental Research, Educational, or Technology Advancement Barriers
and the Methodologies Used to Address Them:
The project will advance knowledge on the design of nonvolatile processors and answer the
following fundamental questions:

1) What state of the processor should be saved in non-volatile store?
2) How often and what granularity should state be saved?
3) How should a system apportion available energy to state saving and useful computations?
4) How does non-volatility influence the abilities of health assist platforms?

Any research aspect that involves foreign collaborations, especially indicating the length of time
US faculty or students spent abroad conducting their work, and vice versa, and the value added of
that work to the student’s/faculty’ work:

The project will leverage ongoing collaborations between Prof. Narayanan and Prof. Huazhong
Yang and Prof. Yongpan Liu in Tsinghua University. The non-volatile processor design and
research in this platform has already been supported by China government foundations including
NSFC and the National Science and Technology Major Project, as well as international industrial
companies such as ROHM (Japan), Huawei. A second-generation is also being developed with
improved computation performance, power-efficiency, turning-on/off time, and supporting
interface that could be integrated into this platform in the future. The goal is for this research to
influence further enhancements to the microarchitecture and system architecture to support the
shared goals of ASSIST and the researchers in Tsinghua to improve wellness and health. Prof.
Narayanan and Prof. Liu had exchange visits lasting a week each. Student Kaisheng Ma also spent
a week at Tsinghua working on prototype.

Achievements in Year 3 and Previous Years:
1. The project explored the architectural space for ambient energy harvesting nonvolatile
processors, and part of this work has been accepted by the 21st IEEE Symp. on High Performance
Computer Architecture (HPCA) and has received the Best paper nomination. The contribution of
this work includes various aspect of the architecture exploration for ambient energy harvesting
nonvolatile processors:

   Architectures were explored that optimize energy-harvesting processors with different
complexities, depending on the nature of the energy source and application characteristics.

   We demonstrate a simulation infrastructure combining Register-Transfer-Level (RTL) and
analytical models to evaluate the optimal architecture from a performance and an energy
perspective. Figure 2 shows the simulation platform details. In the platform, non-volatile processor
architecture simulations will be carried out, and real-time harvester power will be applied as the
input power constraints. We will use various sensor processing algorithms (such as ExG analysis)
to study effect of workloads. NVSim is also used to provide timing, power, and area specifications
for various types of available non-volatile memory. With all the data above, we carry out the
architectural-level simulations based on synthesizable Verilog using Synopsys Modelsim. We
explore various architectural-level optimization methods. With the Cadence tools, we will be able to evaluate the power and area performance for the system. In the second step, peripheral interfaces like IIC, SPI, RS-232 etc. will be added into the system simulation and verification. EEG/ECG sensors, amplifiers, and A/D converters will also be included together with the EEG/ECG self-diagnosing algorithms.

An evaluation was carried out of a fabricated NVP chip to calibrate our simulation model. This NVP chip is a non-volatile ferroelectric processor THU1010N that is designed by Tsinghua University based on the ferroelectric flip-flops from Rohm Co. Ltd. It has highlighted characteristics of instant turning-on/off within micro seconds, zero standby power and resilience to power failures occurring at even 20 KHz. It integrates a standard 8051 micro-controller to support general instructions and a reconfigurable voltage detection system for automatic system backup during power failures.

We propose several policies that tradeoff between performance and the utilization of available energy by choosing which data to save, and when to save it.

![Simulation Platform Diagram](image1)

**Figure 2. Simulation platform**

![Self-power Health System Diagram](image2)

**Figure 3. Self-power health system using nonvolatile logic and memory.**

2. A prototype system was designed to demonstrate the utility of the non-volatile logic and memory in self-powered health systems, as shown in Figure 3.
Summary of other relevant work being conducted within and outside of the ERC and how this project is different:
The study of architectural aspects of non-volatile processor has initiated a completely new focus on energy-scavenged systems. The novelty of this work is well reflected in the best paper nomination at the premier architecture conference. However, the aspects of this work are very relevant to the design of energy-harvested health care systems being developed by various researchers in ERC and outside, especially with battery-less systems.

Plans for next year:
In the next year, we will continue the work in two aspects:
1. We will continue using the emerging devices including TFETs and Ferroelectric FETs to design energy-efficient and/or nonvolatile circuits so as to deal with unstable intermittent ambient energy supply; we’ll explore the use of nonconventional logic architecture to bring new features such as energy efficiency, non-volatility, re-configurability, etc.
2. We will continue to refine the nonvolatile processors proposed in the HPCA in the past year. New system architectures together with new power management policies will be applied.
3. We will continue working on the nonvolatile platform design to support various sensors and signal processing functions.
4. We will continue working with the ASSIST researchers to integrate ASSIST energy harvesters to power the nonvolatile health platform.

Expected milestones and deliverables for the project:
Goal 1:
- Complete design of policies for power management to incorporate to prototype platform (February 28, 2015)
- Validate and refine simulator based on prototype studies and to reflect ASSIST technology enhancements May 1, 2015
- New logic architecture based on emerging devices, either for high power efficiency, nonvolatility, or reconfigurability (August 1, 2015)
- Design of 2nd version nonvolatile processor that incorporates new techniques that were proposed in our previous paper in 2015 (October 1, 2015)
- Performance evaluation of the 2nd version processor (December 1, 2015)

Goal 2:
- Complete sensor interface design (February 28, 2015)
- Complete software mapping on non-volatile processor (May 1, 2015)
- Complete system ready for demonstration (May 15, 2015)
- Test environment of the 2nd version nonvolatile processor (October 31, 2015)
- Health platform design using the 2nd version nonvolatile processor (December 31, 2015)

Member Company Benefits:
Technology should be of importance to many member companies.

Commercialization Impacts or Course Implementation Information: N/A